INSTITUT D'ELECTRONIQUE ET DE TELECOMMUNICATIONS DE RENNES

Reliability Improvement in Reconfigurable FPGAs

B. Chagun Basha

Jeudis de la Comm
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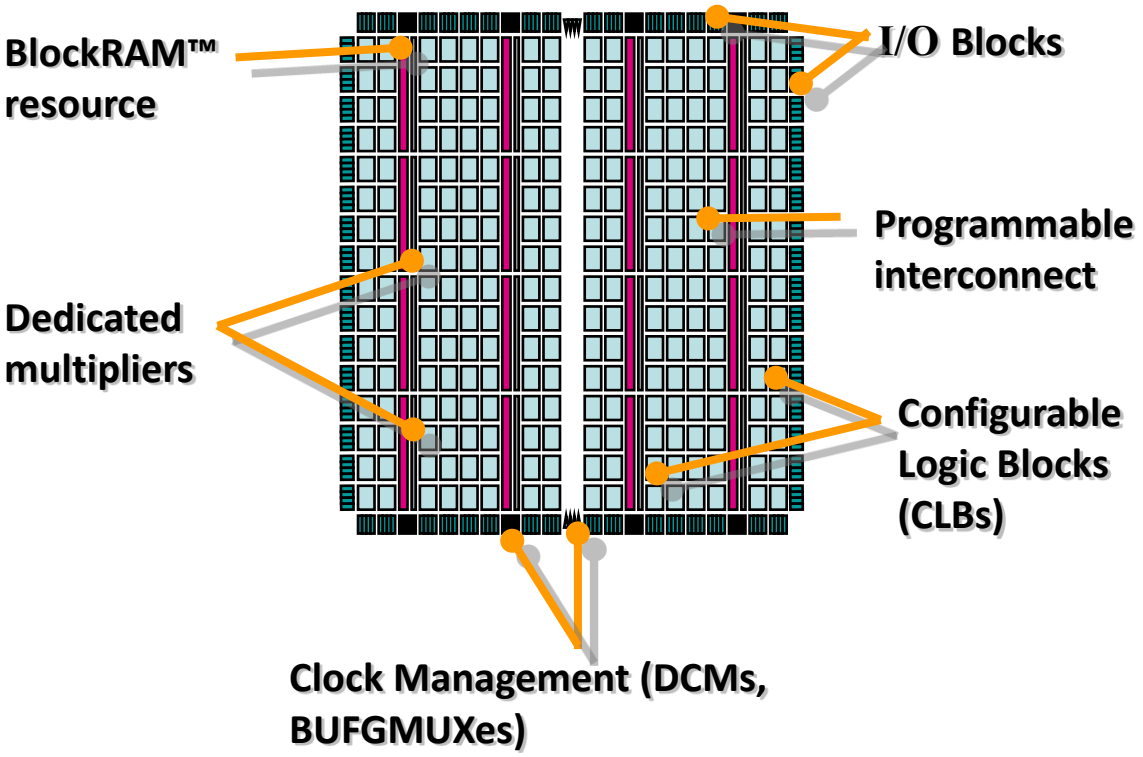
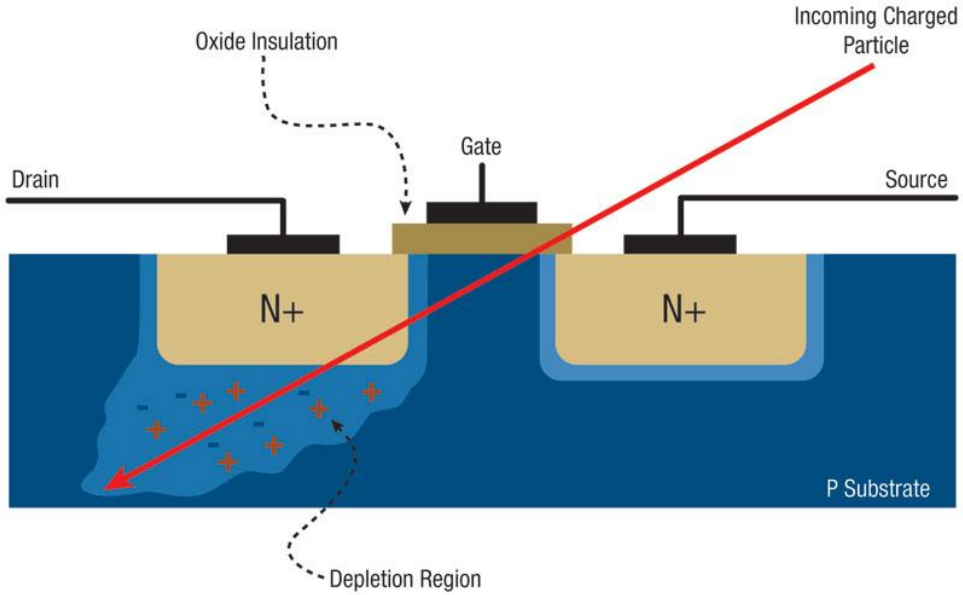
Overview

FPGA Fabrics



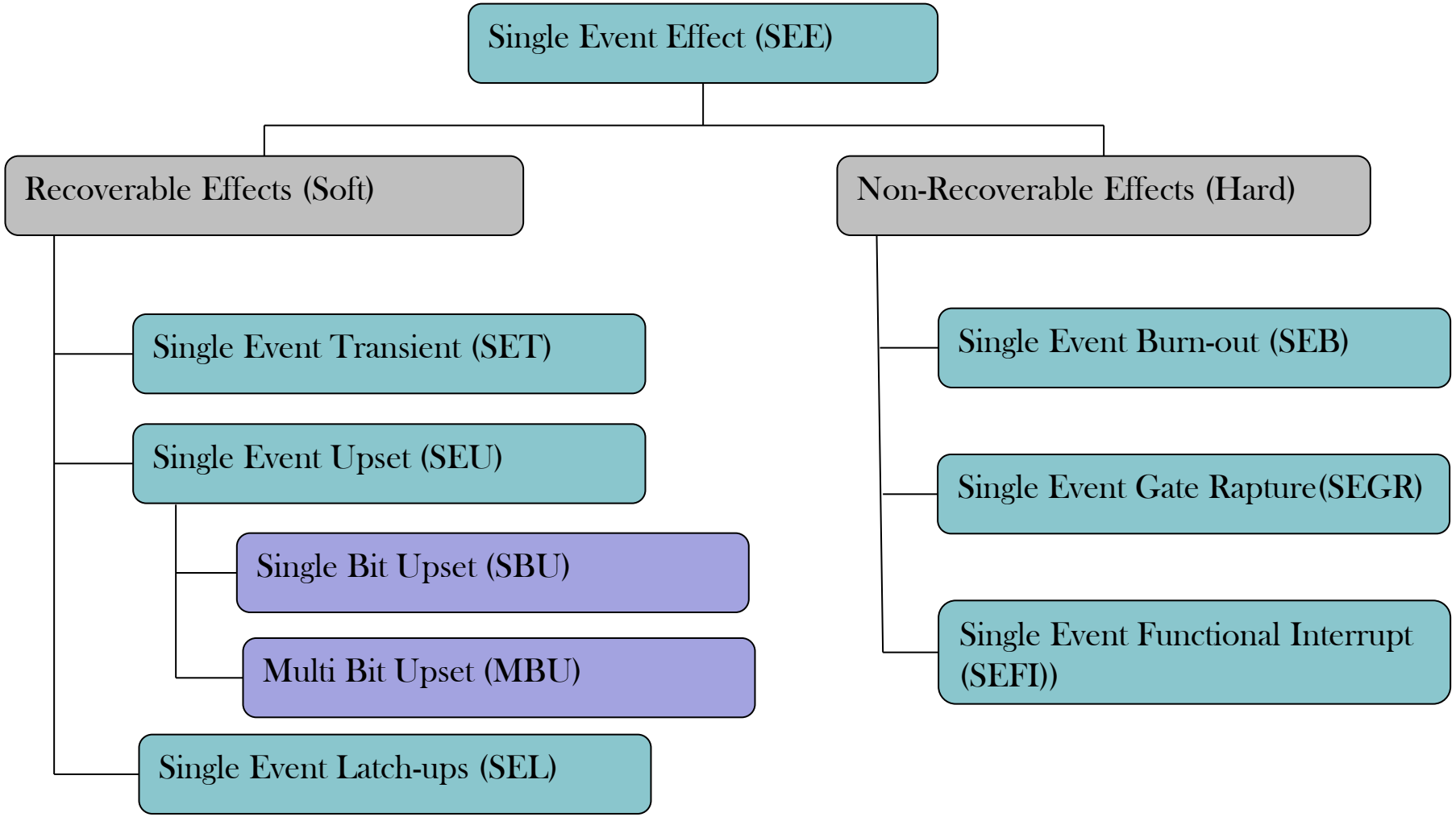
- **Logic Resources**
  - Combinational
  - Sequential
- **Configuration Bitstream**
  - SRAM

Single Event Effects [2]



Single Event Effects (SEE) occur when a high-energy particle passes through the active region of a semiconductor, triggering non-destructive effects such as upset, multiple-bit upset, or analog transients; or destructive effects such as latch-up, gate rupture, and burnout.

Designing with Dependability



Designing with Dependability

Logic Resources

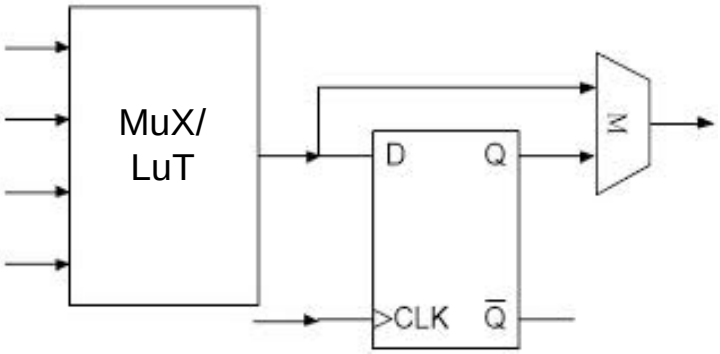
Mux/LuT

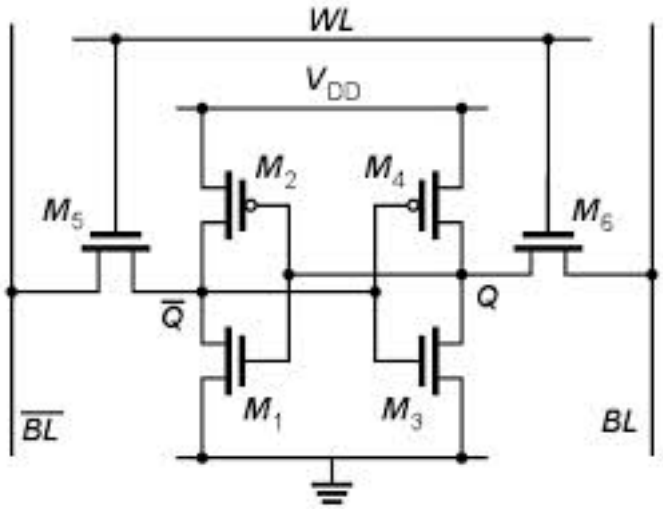
D-FF

Configuration Bitstream

SRAM

- Combinational as well as Sequential functional Implementation.





Reliability Improvement

Configuration Bitstream Protection

- Single Event Upset (SEU)
  - Single Bit Upset (SBU)
  - Multi Bit Upset (MBU)

Solution

✓ Built-in 3D-Hamming Multiple Error Correcting Scheme.

Logic Resources Protection

Transistor Fault Model :

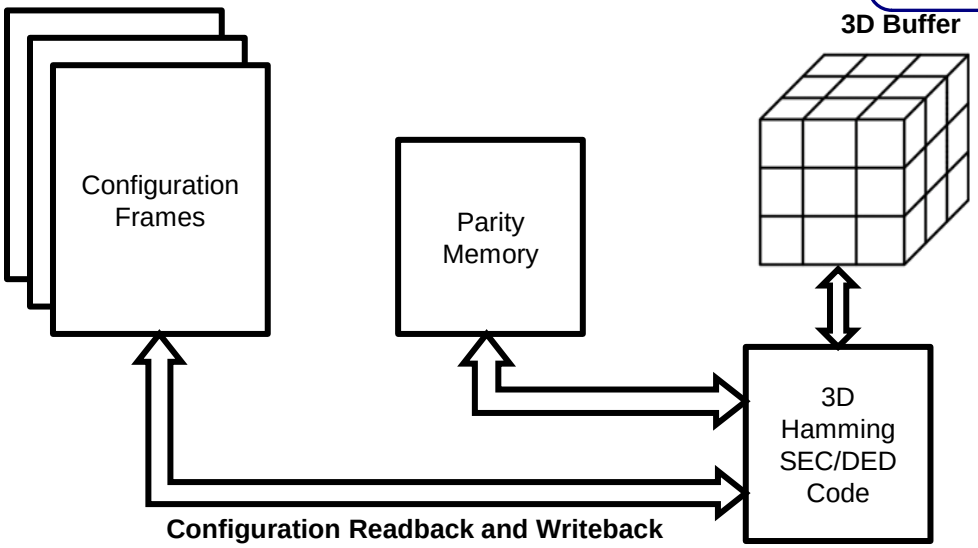
- Stuck faults (1, 0, close, open)
- Bridging between signal lines (i/p , o/p)
- Shorts in Source-Drain (SD), Gate-Source (GS), & Gate-Drain (GD)

Solution

?!

✓ This is what the presentation talks about.

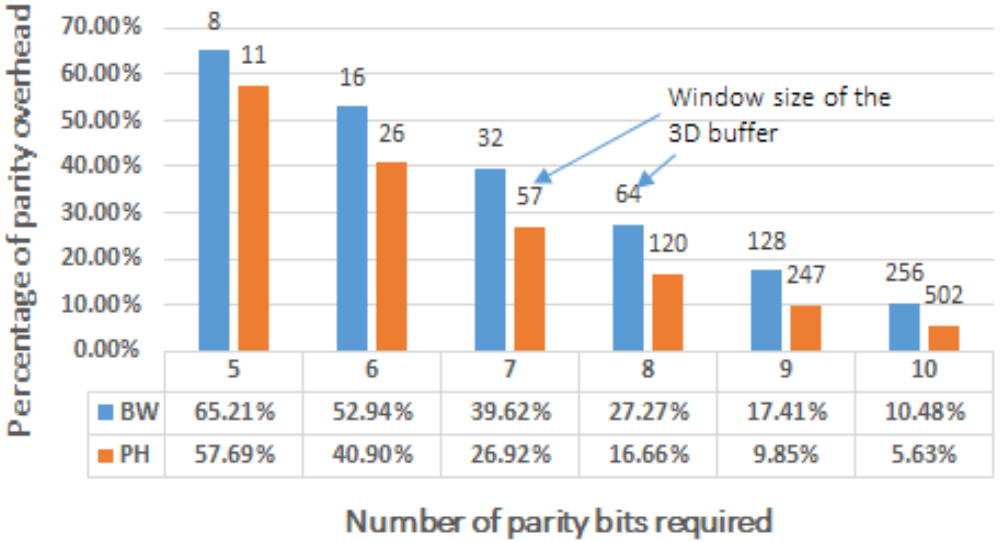
Built-in 3D-Hamming EC Scheme



Reference : Chagun Basha, Sébastien Pillement and Stainslaw Piestrak, 'Built-in 3-Dimentional Hamming Multiple-Error Correcting Scheme to Mitigate Radiation Effects in SRAM-Based FPGAs', ARC'14 April 2014, Portugal.

- Built-in protection
- Less parity memory overhead
- Improved Multiple bit error correcting capability.

Optimization of Parity Memory Overhead

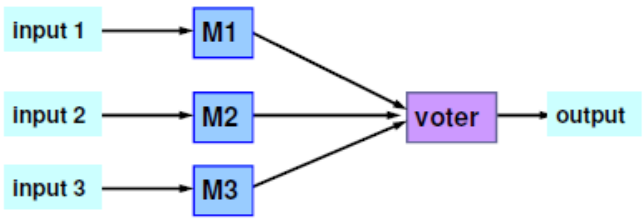


Logic Resource Protection

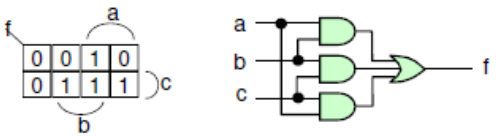
- Passive Redundancy Techniques
  - Fault Masking
- Active Redundancy Techniques
  - Detection, Localization, Recovery
- Hybrid Redundancy Techniques
  - Fault Masking/Detection + Reconfiguration (Dy-Pr)

Are they focus really on Logic Fault Models ?

Triple Modular Redundancy (TMR)

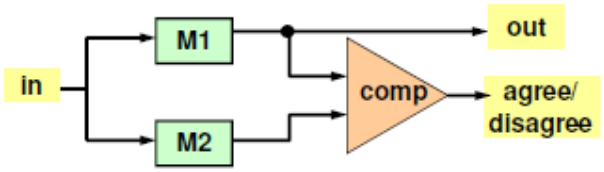


f = ab + ac + bc



n-bit majority voter: n times 1-bit

Duplication with Comparison (DWC)



- Pair and a spare
- Watch dog –Lock step
- Standby sparing
- Concurrent detection

Hybrid

Redundancy

- Fault detection and masking

+

Reconfiguration

- Recovery

Concept of Totally Self-Checking Circuits (TSC) [3]

A circuit is **totally self-che**cking if it is both **fault secure** and **self-testing**.

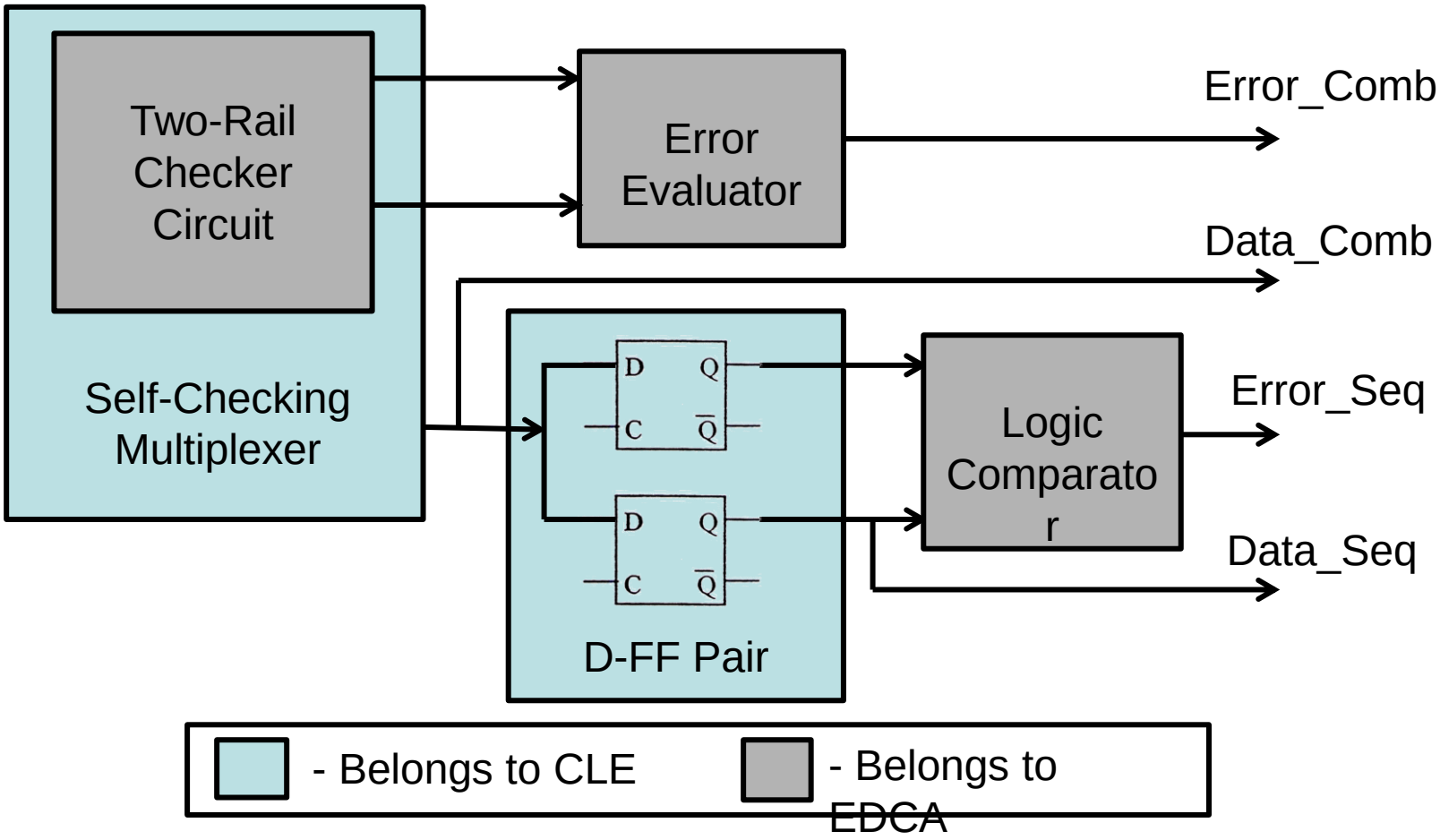
- ✓ Totally self-checking circuits are very desirable for highly reliable system design.
- ✓ Such circuits have significant advantages, such as:

(1) Transient faults as well as permanent faults are detected.

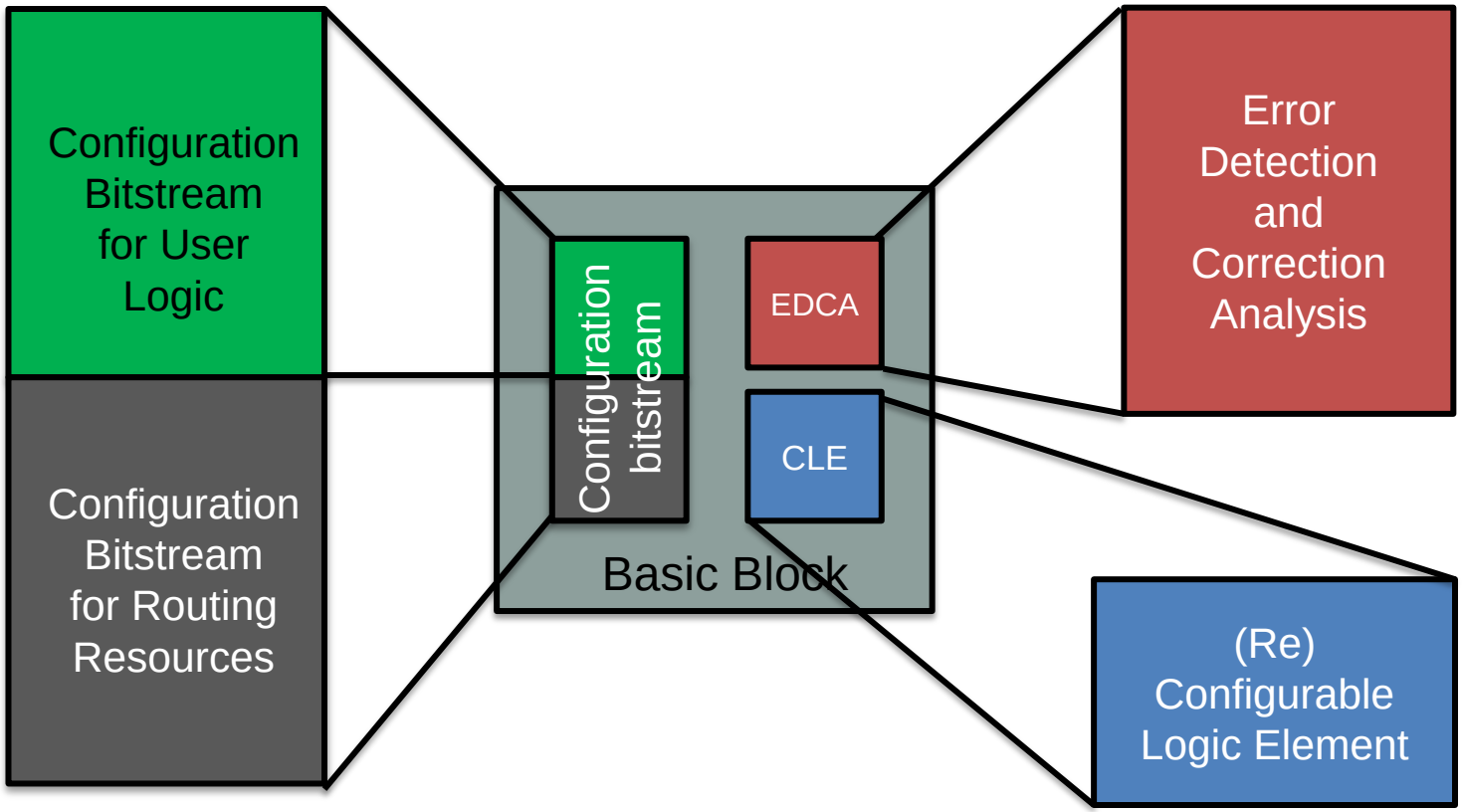
(2) Faults are immediately detected upon occurrence; this prevents propagation of corrupt data within the system.

Self Checking Circuits deals with "**Logic Faults"**

Block Diagram of Proposed Self-Checking Logic Block



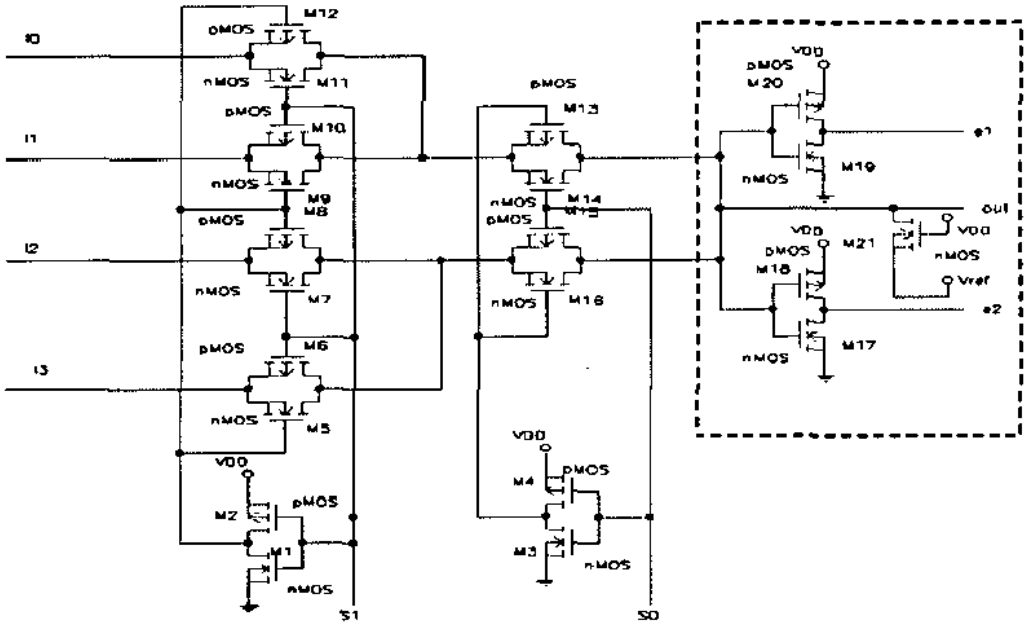
Basic Building Block



Self- Checking Multiplexers

In [4], a new Two-Rail Checker (TRC) circuit is presented, to detect the presence of logic faults such as bridging and stuck-on.

Inspired by the TRC presented in [4], a new Fault Tolerant Multiplexer is proposed in [5] & [6].



2. Self-Checking Multiplexer design [5]

1. Two-Rail Checker

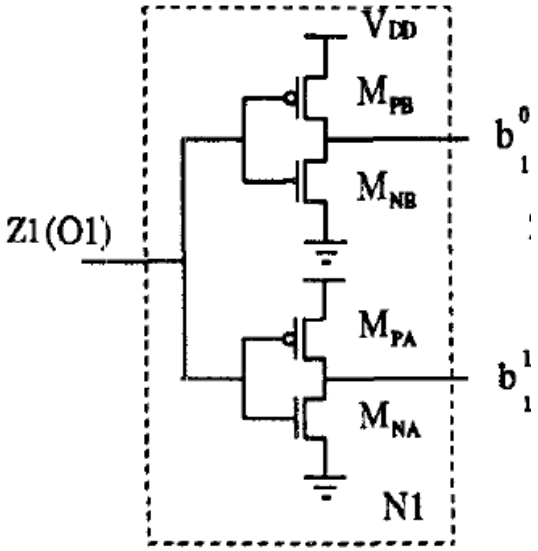
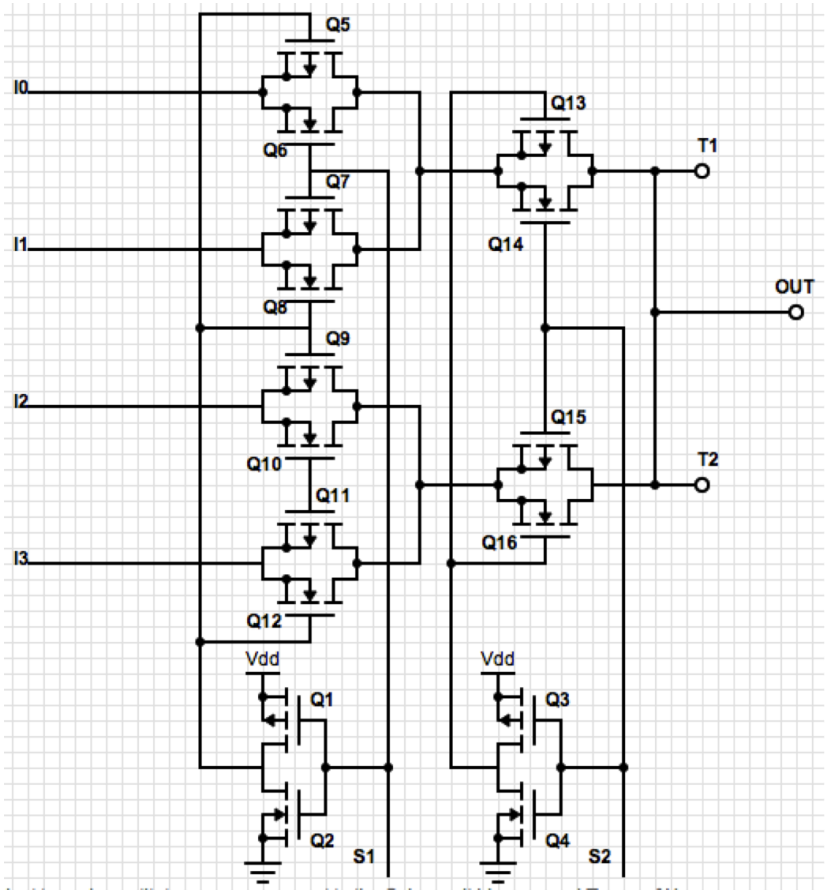
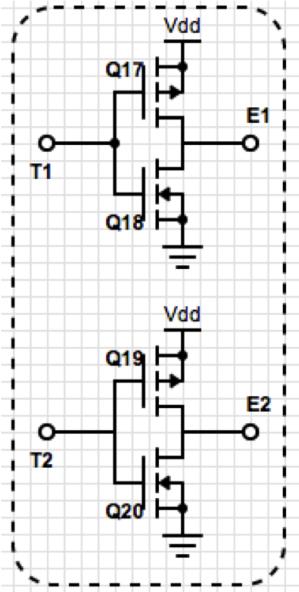


Fig 2 shows how to check a **4** input multiplexer by adding two inverters (M17M18 and M19M20) to its output(out).

Proposed Self-Checking Multiplexer

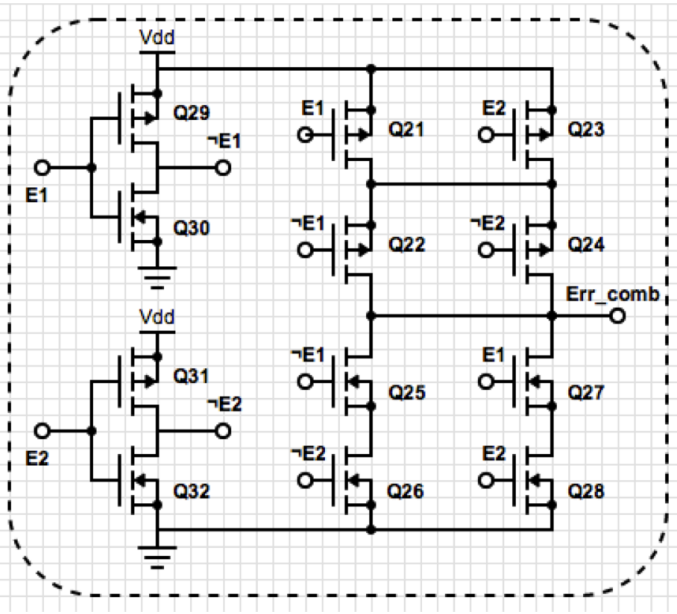


Multiplexer Functional Circuit



Different Threshold Voltage
Inv (Q17/Q18) – V_{T1}
Inv (Q19/Q20) – V_{T2}

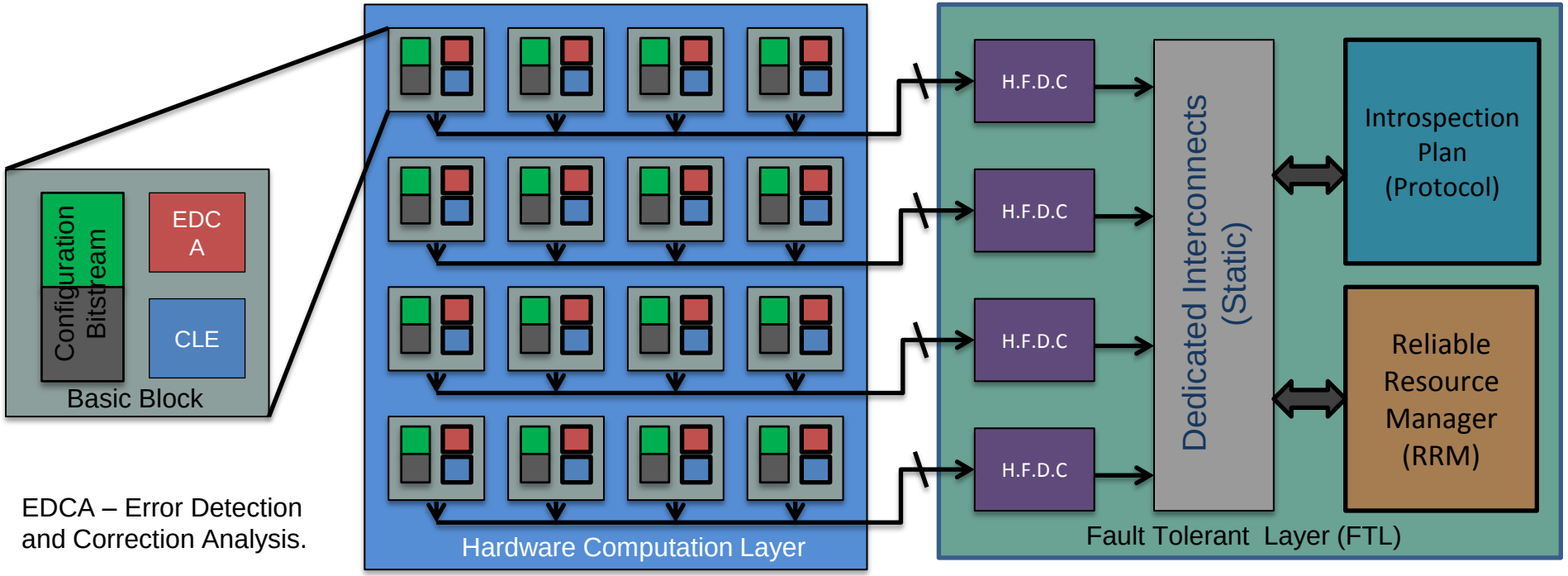
Two Rail Checker



E1	E2	Err_comb
0	0	Fault Free
0	1	Fault
1	0	Fault
1	1	Fault Free

Error Evaluator

ARDyT© FPGA Architecture



EDCA – Error Detection and Correction Analysis.

CLE – Configurable Logic Element.

Basic Building Block Cluster

*H.F.D.C – Hierarchical Fault Detection Chain

Hardware Overhead Comparison

		Protection Scheme			
		Proposed Scheme	Proposed Scheme (With Unused Internal FF)	Dual Modulo Redundancy (DMR)	Triple Modulo Redundancy (TMR)
Logic Cell	4-Input	186 %	148 %	226 %	356 %
	8-Input	150 %	130 %	215 %	332 %

Table 2: Hardware overhead comparison of fault tolerant logic cell architectures

References

1. Study of an architecture for fault tolerant Field Programmable Gate Arrays http://www.dspvlsi.uniroma2.it/index.php/it/attivita/66-past-projects/80-study-of-an-architecture-for-fault-tolerant-field-programmable-gate-arrays.html?showall=&start=1
2. Martha O'Bryan, Single Event Effects : Radiation Effects and Analysis, http://radhome.gsfc.nasa.gov/radhome/see.htm
3. [Book] Self-checking and Fault-tolerant Digital Design By Parag K. Lala, Academic Press, 2001 UK.
4. Cecilia Metra, Michele Favalli, Piero Olivo, Bruno Riccb, CMOS Checkers with Testable Bridging and Transistor Stuck-on Faults, International Test Conference 1992, pp 948-957.
5. S. *Pontarelli,* G.C. *Cardarilli, A. Leandri, M Ottavi, M Re. A. Salsano,* A Self-checking Cell Logic Block for Fault Tolerant FPGAs, Department of Electronic Engineering University of Rome "Tor Vergata", Italy, 2002.
6. Dilip P. Vasudevan, Parag K. Lala, and James Patrick Parkerson, Self-Checking Carry-Select Adder Design Based on Two-Rail Encoding, IEEE Transactions on Circuits and Systems - Vol. 54, No. 12, Dec 2007.
7. S.M.Kia, S. Parameswaran, Designs for self checking flip-flops, *IEE Proc.-Comput. Digit. Tech., Vol. 145, No. 2, March 1998.*